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VIII. (B) All of the claims presented in the above-identified patent application are believed to be directed to a single invention. If the Examiner believes that the pending claims are directed to more than one invention, Applicants hereby agree to elect claims directed to a single invention, without traverse.

The present invention is directed to a method and system for routing in decoders for low density parity check (LDPC) codes. LDPC codes are a class of block error control codes that allow a communication system to approach the Shannon limit, which is the theoretical upper limit for data rate at a given signal to noise ratio. However, LDPC codes have not been widely deployed commercially because of their complexity and because very large blocks are required for effective use, thus causing storage problems. Therefore, it is an objective of the present invention to provide an approach for decoding structured LDPC codes to be used in a communication system that efficiently uses the LDPC codes to support high data rates without introducing greater complexity and that minimizes storage requirements.

The present invention addresses this objective by providing a combination of method and structure for decoding LDPC-coded signals that retrieves edge values associated with a structured parity check matrix used to generate the LDPC-coded signal, wherein the edge values specify relationships between bit nodes and check nodes, and wherein the edge values are stored according to a predetermined scheme that permits concurrent retrieval of a set of edge values. The predetermined scheme preferably specifies contiguous physical memory locations for the set of edge values.

VIII. (C) A pre-examination search was conducted by a professional search firm. The search was conducted in Class 375, subclasses 261, 265, 268, 269, 272, 279, and 286; Class 714, subclasses 752, 758, 777, and 781; and on computer using Delphion, EPO ESPACE, and PTO databases; and on the Internet. In addition, an International Search Report for corresponding International Patent Application No. PCT/US03/21071 has been issued by the European Patent Office acting as the International Search Authority.

VIII. (D) The pre-examination search revealed the following references:

- (i) U.S. Patent Application Publication No. US 2003/0104788 A1
- (ii) U.S. Patent Application Publication No. US 2003/0074626 A1
- (iii) U.S. Patent Application Publication No. US 2003/0023917 A1
- (iv) Mansour et al., "Low-Power VLSI Decoder Architectures for LDPC Codes", Proceedings, IEEE International Symposium on Lower Power Electronics and Design, pp. 284-289, August 12-14, 2002

Each of these references is included in the Information Disclosure Statement, along with a copy of each reference.

The International Search Report cited the following additional references:

- (v) International Publication No. WO 02/103631 A1
- (vi) T. Zhang et al., "Joint Code and Decoder Design for Implementation-Oriented (3,k)-Regular LDPC Codes", Proceedings, 35th Asilomar Conference on Signals, Systems, & Computers, pp. 1232-1236, November 4-7, 2001
- (vii) E. Boutillon et al., "Decoder-First Code Design", Proceedings, International Symposium on Turbo Codes and Related Topics, pp. 459-462, September 4-7, 2000
- (viii) G. Al-Rawi et al., "Optimizing the Mapping of Low-Density Parity Check Codes on Parallel Decoding Architectures", Proceedings, IEEE Conference on Information Technology: Coding and Computing, pp. 578-586, April 2-4, 2001
- (ix) A. Selvarathinam et al., "A Massively Scaleable Decoder Architecture for Low-Density Parity-Check Codes", Proceedings, IEEE International Symposium on Circuits and Systems, Vol. 2, pp. 61-64, May 25-28, 2003

Each of these references is included in the Information Disclosure Statement, along with a copy of each reference. A copy of the International Search Report is also included with the Information Disclosure Statement.

VIII. (E) A discussion of the above-listed references is provided below:

(i) United States Patent Application Publication No. US 2003/0104788 A1 relates to architectures for decoding low density parity check codes that permit varying degrees of hardware sharing to balance throughput, power consumption, and area requirements. The LDPC decoding architectures may be useful in a variety of communication systems in which throughput, power consumption, and area are significant concerns. The decoding architectures implement an approximation of the standard message passing algorithm used for LDPC decoding, thereby reducing computational complexity. Instead of a fully parallel structure, this approximation permits at least a portion of the message passing structure between check and bit nodes to be implemented in a block-serial mode, thus providing reduced area without substantial added latency.

In contrast to the present invention, United States Patent Application Publication No. US 2003/0104788 A1 fails to disclose a combination of method and structure for decoding LDPC-coded signals that retrieves edge values associated with a structured parity check matrix used to generate the LDPC-coded signal, wherein the edge values specify relationships between bit nodes and check nodes, and wherein the edge values are stored according to a predetermined scheme that permits concurrent retrieval of a set of edge values, and wherein the predetermined scheme preferably specifies contiguous physical memory locations for the set of edge values.

(ii) United States Patent Application Publication No. US 2003/0074626 A1 relates to a method for decoding LDPC codes that comprises executing a sum product algorithm to recover a set of information bits from an LDPC code represented as a bipartite graph of symbol nodes and check nodes, the sum product algorithm being responsive to input log likelihood ratios associated with the symbol nodes. The check nodes are updated by generating a set of forward difference metrics and a set of backward difference metrics in dependence on the ratios of logarithmic probabilities each associated with a corresponding symbol node of the LDPC code, updating each metric in the set of forward difference metrics in dependence on the absolute value of the log likelihood

ratio associated with the symbol node and the absolute value of the previous metric in the set, updating each metric in the set of backward difference metrics in dependence on the absolute value of the log likelihood ratio associated with the symbol node and the absolute value of the previous metric in the set, and generating log likelihood ratios to be propagated back to each symbol node in dependence on the updated sets of forward and backward difference metrics.

In contrast to the present invention, United States Patent Application Publication No. US 2003/0074626 A1 fails to disclose a combination of method and structure for decoding LDPC-coded signals that retrieves edge values associated with a structured parity check matrix used to generate the LDPC-coded signal, wherein the edge values specify relationships between bit nodes and check nodes, and wherein the edge values are stored according to a predetermined scheme that permits concurrent retrieval of a set of edge values, and wherein the predetermined scheme preferably specifies contiguous physical memory locations for the set of edge values.

(iii) United States Patent Application Publication No. US 2003/0023917 A1 relates to techniques for implementing message passing decoders, for example, LDPC decoders. To facilitate hardware implementation, messages are quantized to integer multiples of one-half of the natural logarithm of 2. Messages are transformed between more compact variable and less compact constraint node message representation formats. The variable node message format allows variable node message operations to be performed through simple additions and subtractions, while the constraint node representation allows constraint node message processing to be performed through simple additions and subtractions. Variable and constraint nodes are implemented using an accumulator module, subtractor module, and delay pipeline. The accumulator module generates an accumulated message sum. The accumulated message sum for a node is stored and then delayed input messages from the delay pipeline are subtracted therefrom to generate output messages. The delay pipeline includes a variable delay element, thus making it possible to sequentially perform processing operations corresponding to nodes of different degrees.

In contrast to the present invention, United States Patent Application Publication No. US 2003/0023917 A1 fails to disclose a combination of method and structure for decoding LDPC-coded signals that retrieves edge values associated with a structured parity check matrix used to generate the LDPC-coded signal, wherein the edge values specify relationships between bit nodes and check nodes, and wherein the edge values are stored according to a predetermined scheme that permits concurrent retrieval of a set of edge values, and wherein the predetermined scheme preferably specifies contiguous physical memory locations for the set of edge values.

(iv) The article entitled "Low-Power VLSI Decoder Architectures for LDPC Codes" by Mansour et al. relates to an LDPC code and LDPC decoder that are jointly designed to induce the structural regularity needed for a reduced-complexity parallel decoder architecture. The authors have recognized that iterative decoding of LDPC codes using the message-passing algorithm have proven to be extraordinarily effective compared to conventional maximum-likelihood decoding, but that the lack of any structural regularity in these codes is a major challenge for building a practical low-power LDPC decoder. The interconnect-driven code design approach presented in this article eliminates the need for a complex interconnection network while still retaining the algorithmic performance promised by random codes. Moreover, a new approach is proposed for computing reliability metrics based on the BCJR algorithm that reduces the message switching activities in the decoder compared to existing approaches. Simulations show that the proposed approach results in power savings of up to 85.64% over conventional implementations.

In contrast to the present invention, the article entitled "Low-Power VLSI Decoder Architectures for LDPC Codes" fails to disclose a combination of method and structure for decoding LDPC-coded signals that retrieves edge values associated with a structured parity check matrix used to generate the LDPC-coded signal, wherein the edge values specify relationships between bit nodes and check nodes, and wherein the edge values are stored according to a predetermined scheme that permits concurrent

retrieval of a set of edge values, and wherein the predetermined scheme preferably specifies contiguous physical memory locations for the set of edge values.

(v) International Publication No. WO 02/103631 A1 relates to methods and apparatus for decoding code words using message passing decoding techniques which are particularly well suited for use with LDPC codes and long code words. The described methods allow decoding graph structures which are largely comprised of multiple identical copies of a much smaller graph. Copies of the smaller graph are subject to a controlled permutation operation to create the larger graph structure. The same controlled permutations are directly implemented to support message passing between the replicated copies of the small graph. Messages corresponding to individual copies of the graph are stored in a memory and accessed in sets, one from each copy of the graph, using a SIMD read or write instruction. The graph permutation operation may be implemented by simply reordering messages, for example, using a cyclic permutation operation, in each set of messages read out of a message memory so that the messages are passed to processing circuits corresponding to different copies of the small graph.

In contrast to the present invention, International Publication No. WO 02/103631 A1 fails to disclose a combination of method and structure for decoding LDPC-coded signals that retrieves edge values associated with a structured parity check matrix used to generate the LDPC-coded signal, wherein the edge values specify relationships between bit nodes and check nodes, and wherein the edge values are stored according to a predetermined scheme that permits concurrent retrieval of a set of edge values, and wherein the predetermined scheme preferably specifies contiguous physical memory locations for the set of edge values.

(vi) The article entitled "Joint Code and Decoder Design for Implementation-Oriented (3,k)-regular LDPC Codes" by Zhang et al. relates to a proposed joint code and decoder design approach to construct a class of (3,k)-regular LDPC codes which exactly fit to a partly parallel decoder implementation. The authors have recognized

that Gallager's LDPC codes have shown excellent performance, and that the decoder hardware implementation is a crucial issue in determining the extent of LDPC applications. The authors have observed that the straightforward fully parallel decoder architecture usually incurs too high a complexity for many practical purposes, and therefore should be transformed to a partly parallel realization. The partly parallel decoder architecture presented in the article is suitable for VLSI implementation, and it has been shown that the jointly developed $(3,k)$ -regular LDPC codes have very good performance.

In contrast to the present invention, the article entitled "Joint Code and Decoder Design for Implementation-Oriented $(3,k)$ -regular LDPC Codes" fails to disclose a combination of method and structure for decoding LDPC-coded signals that retrieves edge values associated with a structured parity check matrix used to generate the LDPC-coded signal, wherein the edge values specify relationships between bit nodes and check nodes, and wherein the edge values are stored according to a predetermined scheme that permits concurrent retrieval of a set of edge values, and wherein the predetermined scheme preferably specifies contiguous physical memory locations for the set of edge values.

(vii) The article entitled "Decoder-First Code Design" by E. Boutillon et al. relates to reversing the sequence order to code design by defining the hardware structure of the decoder and then constructing the code. In a first step a suitable hardware structure is chosen and in the second step, a code is constructed that adequately fits this structure. Thus, by construction, the code is suitable for VLSI implementation. The target is high speed LDPC decoders for which the input symbol and clock rates are equal.

In contrast to the present invention, the article entitled "Decoder-First Code Design" fails to disclose a combination of method and structure for decoding LDPC-coded signals that retrieves edge values associated with a structured parity check matrix used to generate the LDPC-coded signal, wherein the edge values specify relationships between bit nodes and check nodes, and wherein the edge values are stored according to a predetermined scheme that permits concurrent retrieval of a set of

edge values, and wherein the predetermined scheme preferably specifies contiguous physical memory locations for the set of edge values.

(viii) The article entitled "Optimizing the Mapping of Low-Density Parity Check Codes on Parallel Decoding Architectures" by G. Al-Rawi et al. relates to a study of the problem of optimizing the mapping of LDPC codes on parallel machines to minimize the communication cost. To reduce the search space, the problem is solved in two stages: clustering, and cluster allocation. A simplified clustering technique based on a modified min-cut algorithm that reduces the search complexity from $O(n^2)$ to $O(n)$ is proposed. It was found that most of the locality is exploited by the clustering operation, which results in 40%-52% improvement in the total communication cost over random mapping. For large networks, cluster allocation is much more costly and results in only 1%-8% additional improvement in unidirectional and bi-directional torus topologies. The performance of two different approaches for cluster allocation are compared. The first one is based on a min-cut algorithm, and the second one is based on a genetic algorithm. It was found that the min-cut based approach is better for small network sizes. For large network sizes for which the number of clusters is greater than or equal to 64, the genetic based approach becomes more attractive.

In contrast to the present invention, the article entitled "Optimizing the Mapping of Low-Density Parity Check Codes on Parallel Decoding Architectures" fails to disclose a combination of method and structure for decoding LDPC-coded signals that retrieves edge values associated with a structured parity check matrix used to generate the LDPC-coded signal, wherein the edge values specify relationships between bit nodes and check nodes, and wherein the edge values are stored according to a predetermined scheme that permits concurrent retrieval of a set of edge values, and wherein the predetermined scheme preferably specifies contiguous physical memory locations for the set of edge values.

(ix) The article entitled "A Massively Scaleable Decoder Architecture for Low-Density Parity-Check Codes" by A. Selvarathinam et al. relates to a massively scaleable architecture for decoding LDPC codes. This architecture uses hardware scaling and memory partitioning to achieve a throughput of 100 Gbps. Simulation results show that this throughput is achieved without significant bit-error performance degradation.

In contrast to the present invention, the article entitled "A Massively Scaleable Decoder Architecture for Low-Density Parity-Check Codes" fails to disclose a combination of method and structure for decoding LDPC-coded signals that retrieves edge values associated with a structured parity check matrix used to generate the LDPC-coded signal, wherein the edge values specify relationships between bit nodes and check nodes, and wherein the edge values are stored according to a predetermined scheme that permits concurrent retrieval of a set of edge values, and wherein the predetermined scheme preferably specifies contiguous physical memory locations for the set of edge values.

CONCLUSION

It is respectfully requested that examination of the above-referenced application be advanced in accordance with the provisions of 37 C.F.R. § 1.102 and MPEP 708.02.

Applicants' undersigned attorney may be reached by telephone at (301) 601-7252. All correspondence should continue to be directed to our address given below.

Respectfully submitted,

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